The Fourth Element: Insights into the Memristor

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Abstract— **New developments in nanoelectronics are promising a new generation of computing, which has greater focus on device capabilities. Further to many applications of memristors in artificial intelligence or artificial biological systems, they enable reconfigurable nanoelectronics and also provide new paradigms in application specific integrated circuits (ASIC) and field programmable gate arrays (FPGA). Providing a significant reduction in area and an unprecedented memory capacity and device density are the potential features memristors for Integrated Circuits (IC).**

This work reviews the memristor and its characteristics and provides a SPICE macro-model of the memristors which helps us to develop models for the SPICE based circuit analysis tools like HSpice and Spectre. An insight into the memristor device recalling the quasi-static expansion of Maxwell's equations and a review on Chua's argumentation about the memristor through the electromagnetic theory are also given.

I. Introduction

Based on the Semiconductor Industry Association (SIA) report [1], it is predicted that in 2012 Dynamic Random Access Memory (DRAM) capacity will be around 18 Gbits/cm^2. Interestingly, memristor promises an introduction of an extremely high capacity around 100 Gbits/cm^2 [2]. In contrast to DRAM memory, memristors provide non-volatile operation like flash memories. Hence, such device would continue the legacy of Moore's law for another decade.

Two properties of the memristor attracted much attention. Firstly, its memory characteristic, and, secondly, its nanometer dimensions. The memory property and latching capability enable us to think about new methods for nano-computing. With the nanometer scale device provides a very high density and is less power hungry. In addition, the fabrication process of nano-devices is simpler and cheaper than the conventional CMOS fabrication [3], at the cost of extra device defects [4].

At the architectural level, a crossbar-based architecture appears to be the most promising nanotechnology architecture [5]. Inherent defect-tolerance capability, simplicity, flexibility, scalability, and providing maximum density are the major advantages of this architecture by using a memristor at each cross point.

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Apart from architectural level challenges, this paper focuses on the memristor device and reviews its device level properties. Although the memristor as a device is new, it was conceptually postulated in 1971 by Leon Chua [6]. Chua predicted that a memristor could be realized as a purely dissipative device as a fourth fundamental circuit element. Thirty seven years later, Stan Williams and his group in the Information and Quantum Systems (IQS) Lab at HP realised the memristor in device form [7].

In Section II, we review the memristor and its characteristics as a nano-switch. This section focuses on the memristor, which was realised by Hewlett-Packard (HP) [7] and review its properties based on the early mathematical modeling. Section III presents a preliminary SPICE macro-model of the memristor. Section IV describes an interpretation of the memristor based on electromagnetic theory by recalling Maxwell's equations. Finally, we summarise this review in Section V.

II. Memristor Device and Memrisive System

Traditionally there are only three fundamental passive circuit elements: resistors, capacitors, and inductors. However, one can set up five different mathematical relations between the four fundamental circuit variables: electric current i, voltage v, charge q, and magnetic flux φ. In 1971, Leon Chua, a professor at UC Berkeley, proposed that there should be a fourth fundamental passive circuit element to set up a mathematical relationship between q and φ ($F(q,\varphi)=0$), which he named the *memristor* (a portmanteau of *memory* and *resistor*) [6]. Chua predicted that a class of memristors might be realizable in the form of a pure solid-state device without an internal power supply.

In 2008, Williams et al., at Hewlett Packard, announced the first fabricated memristor device [7]. However, a resistor with memory is not a new thing. If taking the example of non-volatile memory, it dates back to 1910, when Corbino introduced this concept[1]. Later, in 1960, Widrow introduced a new circuit element named the *memistor* [9]. The reason for choosing the name of memistor is exactly the same as memristor. The memistor has three terminals and its resistance is controlled by the time integral of a control current signal. This means that the resistance of the memistor is controlled by charge. However, the memistor is not exactly what the researches were searching for. It is just a charge-controlled three-terminal (transistor) device. Sometimes the memristor

[1] In [8], Chua stated that Corbino's work is one of the first works in this area.

concept is confused with various two-port networks, but basically all of such two-port networks are not memristor according to Chua's paper [6]. Therefore, two-port network resistors, such as gyrators [10] and nullors [11], are not memristors. In addition, as discussed later, one of the best ways to define a memristor in terms of its voltage and current relationship is $v(t) = R(x)i(t)$, where x is the internal state of device. This is one of the most important properties of the memristor.

Chua mathematically predicted that there is a solid-state device, which defines the missing relationship between four basic variables [6]. Recall that a resistor establishes a relation between voltage and current, a capacitor establishes a charge-voltage relation, and an inductor realizes a current-flux relationship, as demonstrated in Fig. 1. Consequently, we have $v = f_{\mathrm{R}}(i)$, $q = f_{\mathrm{C}}(v)$ and $\varphi = f_{\mathrm{L}}(i)$ for a current-controlled resistor, a voltage-controlled capacitor and a current-controlled inductor, respectively. Voltage-controlled resistors, charge-controlled capacitors and flux-controlled inductors also have similar definitions, $i = g_{\mathrm{R}}(v)$, $v = g_{\mathrm{C}}(q)$ and $i = g_{\mathrm{L}}(\varphi)$. Notice that we are specifically discussing nonlinear circuit elements here.

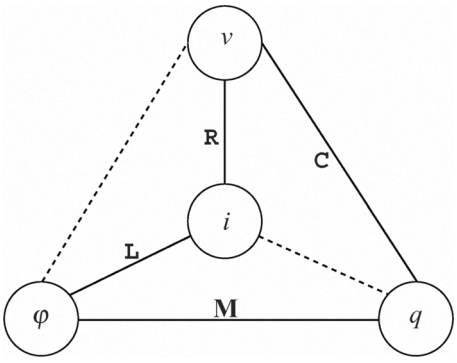

Fig. 1. The four fundamental two-terminal circuit elements. The dashed lines represent $\varphi(t) = \int_{t_0}^{t} v(\tau)d\tau$ and $q(t) = \int_{t_0}^{t} i(\tau)d\tau$ equations. R, C, L and M shows Resistor, Capacitor, Inductor and memristor, respectively (Adapted from [12]).

Consequently, $\varphi = f_{\mathrm{M}}(q)$ $(q = g_{\mathrm{M}}(\varphi))$ defines a charge-controlled (flux-controlled) memristor. Then, $\frac{d\varphi}{dt} = \frac{df_{\mathrm{M}}(q)}{dq}\frac{dq}{dt}$ $(\frac{dq}{dt} = \frac{dg_{\mathrm{M}}(\varphi)}{d\varphi}\frac{d\varphi}{dt})$ which means, $v(t) = \frac{df_{\mathrm{M}}(q)}{dq}i(t)$ $(i(t) = \frac{dg_{\mathrm{M}}(\varphi)}{d\varphi}v(t))$. Note that, $M(q) = \frac{df_{\mathrm{M}}(q)}{dq}$ for a charge-controlled memristor and $W(\varphi) = \frac{dg_{\mathrm{M}}(\varphi)}{d\varphi}$ for a flux-controlled memristor, where $M(q)$ is incremental memristance and $W(\varphi)$ is incremental memductance where the unit of $M(q)$ is Ohm and the unit of $W(\varphi)$ is Siemens [6].

As a matter of fact, $M(q)$ is the slope of the φ-q curve. Hereupon, in a special case of a memristor, for a piecewise φ-q curve with two different slopes, there are two different values for $M(q)$, which is exactly what is needed in binary logic. For detailed information regarding typical φ-q curves the reader is referred to [6].

It is also obvious that if $M(q) \geq 0$, then instantaneous power dissipated by a memristor, $p(i) = M(q)(i(t))^2$ is always positive, so, the memristor is a passive device, and so, φ-q is a monotonically increasing function. This feature is what we exactly see in the HP memristor device. Some other properties of the memristor like zero-crossing between current and voltage signals can be found in [6] and [13]. The most important feature of a memristor is its pinched hysteresis loop v-i characteristic. A very simple consequence of this property and $M(q) \geq 0$ is that such device is purely dissipative like a resistor. Hence, in all cases the energy entering the device is positive.

Another important property of a memristor is its excitation frequency. It has been proven that the pinched hysteresis loop is shrunk by increasing the excitation frequency [13]. In fact, when the frequency increases toward infinity, memristor acts as a linear resistor [13]. Fig. 2 shows both the hysteresis characteristic and frequency response of a memristor [14].

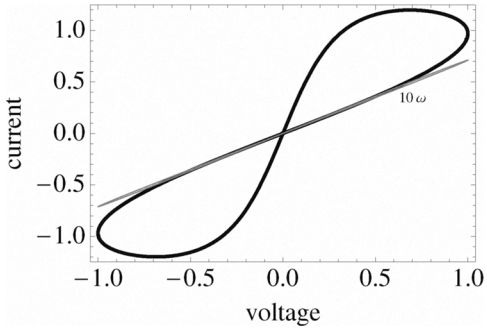

Fig. 2. Pinched hysteresis loop characteristics (After [15])

Interestingly enough, an attractive property of the HP memristor [7], which is exclusively based on its fabrication process, can be deducted from the HP memristor simple mathematical model [7] in Eq. 1.

$$M(q) = R_{\mathrm{OFF}}\left(1 - \frac{R_{\mathrm{ON}}}{\beta}q(t)\right), \qquad (1)$$

where β has the dimensions of magnetic flux $(\varphi(t))$. Here, $\beta = \frac{D^2}{\mu_{\mathrm{D}}}$ in unit of $\mathrm{sV} = \mathrm{Wb}$, where μ_{D} is the average dopant mobility in unit of $\mathrm{cm}^2/\mathrm{sV}$ and D is semiconductor film (titanium dioxide, TiO_2) thicknesses. Note that R_{OFF} and R_{ON} are simply the 'on' and 'off' state resistances as indicated in Fig. 3. Also $q(t)$ defines the total charged passing through the memristor device in a time window, t - t_0. Notice that the memristor has an internal state [13]. Furthermore, as stated in [16], $q(t) = \int_{t_0}^{t} i(\tau)d\tau$, as the state variable in a charge-controlled memristor, gives the charge passing through the device and is not storage charge as in a capacitor. This concept is very important from two points of view. First of all, a memristor is not an energy-storage element. Second, this shows that memristor is not merely a nonlinear resistor but is a nonlinear resistor with charge as a state variable [16].

Five years after the Chua's paper on the memristor [6], he and his graduate student, Kang, published a paper defines a much broader class of systems, named *memristive systems*. From the memristive systems view point a generalized definition of a memristor would be $v(t) = R(w)i(t)$, where

w defines the internal state of the system and $\frac{dw}{dt} = f(w,i)$ [13]. Based on this definition a memristor is a special case of memristive systems.

HP memristor [7] can be defined based on memristive systems. They used a very thin film TiO_2 sandwiched between two Platinum (Pt) contacts and doped one side of the TiO_2 with oxygen vacancies, which are positively charged ions. Therefore, there are two thin films, one is doped and the other is undoped. Such a doping process makes two different resistances: one is high resistive (undoped) and the other is low resistance (doped). Hence, intentionally HP established a device that is illustrated in Fig. 3. The internal state variable, w, is also the variable length of the doped region. Roughly speaking, when $w \to 0$ we have nonconductive channel and when $w \to D$ we have conductive channel. The HP memristor switching mechanism is further discussed in [17].

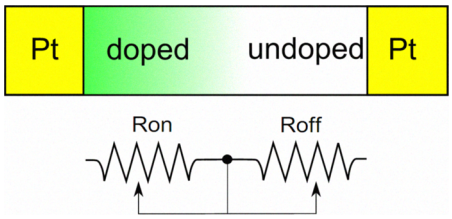

Fig. 3. HP memristor with a simplified equivalent circuit. (Adapted from [7])

The following equation for w is at the heart of the HP memristive system mechanism [15], [18]:

$$\frac{1}{D}\frac{dw(t)}{dt} = \frac{R_{ON}}{\beta} i(t) \ , \tag{2}$$

Integrating Eq. 2 gives $\frac{w(t)}{D} = \frac{w(t_0)}{D} + \frac{R_{ON}}{\beta} q(t)$, where $w(t_0)$ is the initial length of w. Hence, the speed of drift under a uniform electric field across the device is given by $v_D = \frac{dw(t)}{dt}$. In uniform field we have $D = v_D \times t$. In this case $Q_D = i \times t$ also defines the amount of required charge to move the boundary from $w(t_0)$ $(w \to 0)$ to distance $w(t_D)$ $(w \to D)$. Therefore, $Q_D = \frac{\beta}{R_{ON}}$, so

$$\frac{w(t)}{D} = \frac{w(t_0)}{D} + \frac{q(t)}{Q_D} \ . \tag{3}$$

If $x(t) = \frac{w(t)}{D}$ then

$$x(t) = x(t_0) + \frac{q(t)}{Q_D} \ , \tag{4}$$

where $\frac{q(t)}{Q_D}$ describes the amount of charge that is passed through the channel over the required charge for a conductive channel.

Using [7] we have,

$$v(t) = \left(R_{ON} \ \frac{w(t)}{D} + R_{OFF} \left(1 - \frac{w(t)}{D} \right) \right) i(t) \ . \tag{5}$$

Using Eq. 4, Eq. 5 can be rewritten as

$$v(t) = \left(R_{ON} \ x(t) + R_{OFF} \left(1 - x(t) \right) \right) i(t) \ . \tag{6}$$

Now assume that $q(t_0) = 0$ then $w(t) = w(t_0) \neq 0$, and from Eq. 6,

$$M_0 = R_{ON} \left(x(t_0) + r \left(1 - x(t_0) \right) \right) \ , \tag{7}$$

where $r = \frac{R_{OFF}}{R_{ON}}$ and M_0 is the memristance value at t_0. Consequently, the following equation shows memristance at time t,

$$M(q) = M_0 - \Delta R \left(\frac{q(t)}{Q_D} \right) \ , \tag{8}$$

where $\Delta R = R_{OFF} - R_{ON}$. When $R_{OFF} \gg R_{ON}$, $M_0 \approx R_{OFF}$ and Eq. 1 can be derived from Eq. 8.

Substituting Eq. 8 into $v(t) = M(q) i(t)$, when $i(t) = \frac{dq(t)}{dt}$, we have,

$$v(t) = \left(M_0 - \Delta R \left(\frac{q(t)}{Q_D} \right) \right) \frac{dq(t)}{dt} \ . \tag{9}$$

Recall that $M(q) = \frac{d\varphi(q)}{dq}$, so the solution is

$$q(t) = \frac{Q_D M_0}{\Delta R} \left(1 \pm \sqrt{1 - \frac{2\Delta R}{Q_D M_0^2} \varphi(t)} \right) \ . \tag{10}$$

Using $\Delta R \approx M_0 \approx R_{OFF}$, the feasible answer is

$$q(t) = Q_D \left(1 - \sqrt{1 - \frac{2}{Q_D R_{OFF}} \varphi(t)} \right) \ . \tag{11}$$

Consequently, using Eq. 4 if $Q_D = \frac{D^2}{\mu_D R_{ON}}$, so the internal state of the memristor is

$$x(t) = 1 - \left(\sqrt{1 - \frac{2\mu_D}{rD^2} \varphi(t)} \right) \ . \tag{12}$$

Current-voltage relationship in this case would be,

$$i(t) = \frac{v(t)}{R_{OFF} \left(\sqrt{1 - \frac{2\mu_D}{rD^2} \varphi(t)} \right)} \ . \tag{13}$$

In Eq. 13, the inverse square relationship between memristance and TiO_2 thicknesses, D, shows that for smaller values of D, the memristance shows improved characteristics, and because of this reason the memristor imposes a small value of D.

In Eqs. 10-13 the only thing which significantly increases the role of $\varphi(t)$ is lower Q_D. This shows that at the micrometer scale $\frac{1}{R_{OFF} Q_D} = \frac{1}{r\beta} = \frac{\mu_D}{rD^2}$ is negligible and the relationship between current and voltage reduces to a resistor equation.

Substituting $\beta = \frac{D^2}{\mu_D}$ that has the same unit as magnetic flux into Eq. 13, and considering $c(t) = \frac{\varphi(t)}{\beta} = \frac{\mu_D \varphi(t)}{D^2}$ as a normalized variable, we obtain

$$i(t) = \frac{v(t)}{R_{\mathrm{OFF}}\left(\sqrt{1 - \frac{2}{r}c(t)}\right)}, \qquad (14)$$

where $\sqrt{1 - \frac{2}{r}c(t)}$ is called *resistance modulation index* by the authors.

There is also no phase shift between current and voltage signals, which means that the hysteresis loop always crosses to the origin as demonstrated in Fig. 2.

For further investigation, if a voltage, $v(t) = v_0 \sin(\omega t)$, is applied across the device, so magnetic flux would be $\varphi(t) = -\frac{v_0}{\omega}\cos(\omega t)$. The inverse relation between flux and frequency shows that at very high frequencies there is only a linear resistor.

It is worth noting that there are also two other elements with memory named the *memcapacior* and *meminductor*[2]. Chua mathematically postulated that these two elements also could be someday realized in device form [8]. The main difference between these three elements, the memristor, memcapacitor and meminductor is that, the memristor is not a lossless memory device and dissipates energy as heat. However, at least in theory, the memcapacitor and meminductor are lossless devices.

III. SPICE Macro-Model of Memristor

A memristor can be realized by connecting an appropriate nonlinear resistor, inductor, or capacitor across port 2 of an M-R mutator, an M-L mutator, and an M-C mutator, respectively[3] [6]. These mutators and nonlinear circuit elements are realised with a SPICE macro-model (or analog behavioral model of SPICE). The macro circuit model realization of a type-1 M-R mutator based on the first realization of the memristor [6] is shown in Fig. 4.

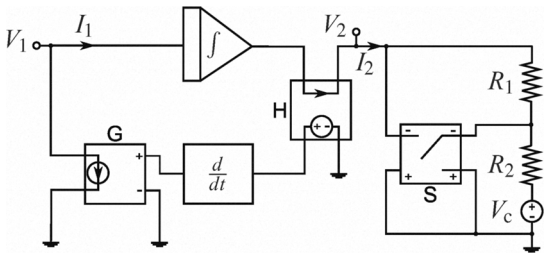

Fig. 4. The SPICE macro-model of memristor. G, H and S are Voltage-Controlled Current Source (VCCS), Current-Controlled Voltage Source (CCVS) and Switch ($V_{\mathrm{ON}} = -1.9$ V and $V_{\mathrm{OFF}} = -2$ V), respectively. $R_1 = R_2 = 1$ kΩ and $V_c = -2$ V.

[2]Memcapacitor (Memcapacitive Systems) and Meminductor (Meminductive Systems) are other concepts that Chua proposed at the first memristor and Memristive Symposium, UC Berkeley [8]. The first explanation of these systems was published in January, 2009 [19].

[3]For further detail about the mutator the reader is referred to [20].

In this model the M-R mutator consists of an integrator, a Current-Controlled Voltage Source (CCVS) "H", a differentiator and a Voltage-Controlled Current Source (VCCS) "G". The nonlinear resistor is also realised with resistors R_1, R_2 and a switch. Therefore, the branch resistance is 1 kΩ for $V < 2$ Volt and 2 kΩ for $V \geq 2$ Volt. The input voltage of port 1, V_1, is integrated and connected to port 2 and the nonlinear resistor current, I_2, is sensed with the CCVS "H" and differentiated and converted into current with the VCCS "G".

SPICE simulations with the macro-model of the memristor are shown in Figs. 5 and 6. The simulated memristor has a value of 1 kΩ when the flux is lower than 2 Wb, but it becomes 2 kΩ when the flux is equal or higher than 2 Wb. The critical flux (φ_c) can be varied with the turn-on voltage of the switch in the macro-model. Fig. 5 shows the pinched hysteresis characteristics of the memristor. The input voltage to the memristor is a ramp with a slope of ± 1 V/s. When the input voltage ramps up with a slope of ± 1 V/s, the memristance is 1 kΩ and the slope of the current-voltage characteristics is 1 mA/V before the the flux reaches to the φ_c. But when the flux becomes 2 Wb, the memristance value is changed to 2 kΩ and the slope is now 0.5 mA/V. After the input voltage reaches to the maximum point, it ramps down and the slope is maintained, because the memristance is still 2 kΩ. Fig. 6 shows the memristor characteristics when a step input voltage is applied. Initially the memristance is 1 kΩ, so the input current is 1 mA. When the flux reaches to 2 Wb (1 V × 2 s), the memristance is 2 kΩ and so the input current is now 0.5 mA as predicted. The developed macro-model can be used to understand and predict the characteristics of a memristor.

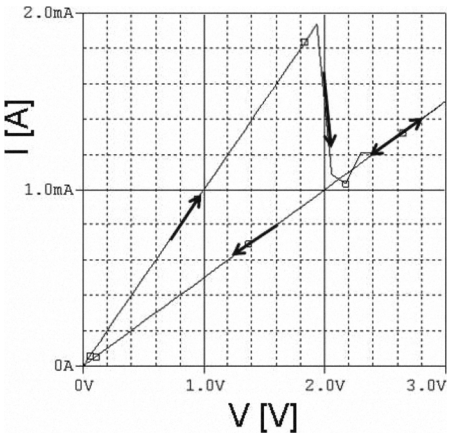

Fig. 5. The hysteresis characteristics of the memristor.

IV. Interpreting Memristor in Electromagnetic Theory

In Chua's original paper [6], he presented an argumentation based on electromagnetic field theory for the existence of the memristor. His motivation was to interpret the memristor in terms of the so-called *quasi-static expansion* of Maxwell's

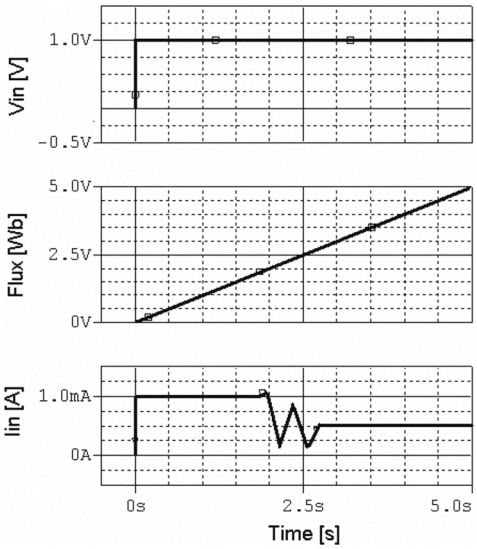

Fig. 6. The memristor characteristics when the step input voltage is applied.

equations. This expansion is usually used to give an explanation to the elements of circuit theory within electromagnetic field theory.

Although Chua's argumentation hints that a memristor might exist, it never proved that this device can in fact be realized physically. In the following we describe how Chua argued for a memristor from a consideration of the quasi-static expansion of Maxwell's equations.

To consider this expansion, we write Maxwell's equations in their differential form as

$$\nabla \times \mathbf{E} = -\frac{\partial \mathbf{B}}{\partial t}, \quad \nabla \times \mathbf{H} = \mathbf{J} + \frac{\partial \mathbf{D}}{\partial t} , \tag{15}$$

where ∇ is the del operator, $\mathbf{E}$ and $\mathbf{H}$ are the electric and magnetic field intensity, $\mathbf{D}$ and $\mathbf{B}$ are the electric and magnetic flux density, and $\mathbf{J}$ is current density.

The idea of a quasi-static expansion involves using a process of successive approximations for time-varying fields. The process allows us to study electric circuits in which time variations of electromagnetic field are slow, which is the case for electric circuits.

Consider an entire family of electromagnetic fields for which the time rate of change is variable. The family of fields can be described by a time-rate parameter α, which is the time rate of change of charge density ρ. We can express Maxwell's equations in terms of the family time $\tau = \alpha t$ and the time derivative of $\mathbf{B}$ can be written as

$$\frac{\partial \mathbf{B}}{\partial t} = \frac{\partial \mathbf{B}}{\partial \tau}\frac{d\tau}{dt} = \alpha \frac{\partial \mathbf{B}}{\partial \tau} , \tag{16}$$

where other time derivatives can be expressed similarly.

In terms of the family time, Maxwell's Eq. 15 takes the form

$$\nabla \times \mathbf{E} = -\alpha \frac{\partial \mathbf{B}}{\partial \tau}, \quad \nabla \times \mathbf{H} = \mathbf{J} + \alpha \frac{\partial \mathbf{D}}{\partial \tau} , \tag{17}$$

which allows us to consider different values of the family time τ corresponding to different time scales of excitation. Note that in Eqs. 17 $\mathbf{E}$, $\mathbf{H}$, $\mathbf{D}$, $\mathbf{J}$, and $\mathbf{B}$ are also functions of α and τ along with the position (x,y,z). This allows us to express [21], for example, $\mathbf{E}(x,y,z,\alpha,\tau)$ as power series in α,

$$\mathbf{E}(x,y,z,\alpha,\tau) = \mathbf{E}_0(x,y,z,\tau) + \alpha \mathbf{E}_1(x,y,z,\tau) + \alpha^2 \mathbf{E}_2(x,y,z,\tau) + ... \tag{18}$$

where

$$\begin{aligned} \mathbf{E}_0(x,y,z,\tau) &= [\mathbf{E}(x,y,z,\alpha,\tau)]_{\alpha=0} \\ \mathbf{E}_1(x,y,z,\tau) &= \left[\frac{\partial \mathbf{E}(x,y,z,\alpha,\tau)}{\partial \alpha}\right]_{\alpha=0} \\ &... \end{aligned} \tag{19}$$

Along with these, similar series expressions for $\mathbf{B}$, $\mathbf{H}$, $\mathbf{J}$, and $\mathbf{D}$ are obtained and can be inserted into Eqs. 17, with the assumption that every term in these series is differentiable with respect to x, y, z, and τ. This assumption permits writing, for example,

$$\nabla \times \mathbf{E} = \nabla \times \mathbf{E}_0 + \alpha(\nabla \times \mathbf{E}_1) + \alpha^2(\nabla \times \mathbf{E}_2) + ... \tag{20}$$

and, when all terms are collected together on one side, this makes Eqs. 17 able to take the form of power series in α that is equated to zero. For example, the first equation in Eqs. 17 becomes

$$\nabla \times \mathbf{E}_0 + \alpha(\nabla \times \mathbf{E}_1 + \frac{\partial \mathbf{B}_0}{\partial \tau}) + \alpha^2(\nabla \times \mathbf{E}_2 + \frac{\partial \mathbf{B}_1}{\partial \tau}) + ... = 0 , \tag{21}$$

which must hold for all α. This can be true if the coefficients of all powers of α are separately equal to zero. The same applies to the second equation in Eqs. 17 and one obtains the so-called nth-order Maxwell's equations, where $n = 0,1,2,....$ For instance, the *zero-order* Maxwell's equations are

$$\nabla \times \mathbf{E}_0 = 0 , \tag{22}$$

$$\nabla \times \mathbf{H}_0 = \mathbf{J}_0 , \tag{23}$$

and the *first-order* Maxwell's equations are

$$\nabla \times \mathbf{E}_1 = -\frac{\partial \mathbf{B}_0}{\partial \tau} , \tag{24}$$

$$\nabla \times \mathbf{H}_1 = \mathbf{J}_1 + \frac{\partial \mathbf{D}_0}{\partial \tau} . \tag{25}$$

The quasi-static fields are obtained from only the first two terms of the power series, Eq. 21, while ignoring all the remaining terms and by taking $\alpha = 1$. In this case we can approximate $\mathbf{E} \approx \mathbf{E}_0 + \mathbf{E}_1$, $\mathbf{D} \approx \mathbf{D}_0 + \mathbf{D}_1$, $\mathbf{H} \approx \mathbf{H}_0 + \mathbf{H}_1$, $\mathbf{B} \approx \mathbf{B}_0 + \mathbf{B}_1$, and $\mathbf{J} \approx \mathbf{J}_0 + \mathbf{J}_1$. Circuit theory, along with

many other electromagnetic systems, can be explained by the zero-order and first-order Maxwell's equations, for which one obtains *quasi-static fields* as the solutions. The three classical circuit elements *resistor*, *inductor*, and *capacitor* can then be explained to be the electromagnetic systems whose quasi-static solutions correspond to certain combinations of zero-order and first-order solutions of Eqs. 22-25.

However, in this quasi-static explanation of circuit elements, an interesting possibility was dismissed [21] as it was thought not to have any correspondence with an imaginable situation in circuit theory. This is the case when both the first-order electric and the first-order magnetic fields are *not* negligible. Chua argued that it is precisely this possibility that provides hints towards the existence a fourth basic circuit element.

Chua's argumentation goes as follows. Assume there exists a two-terminal device in which $\mathbf{D}_1$ is related to $\mathbf{B}_1$, where these quantities are evaluated instantaneously. If this is the case then this device has following two properties:

1) Zero-order electric and magnetic fields are negligible when compared to the first-order fields i.e. $\mathbf{E}_0$, $\mathbf{D}_0$, $\mathbf{B}_0$, and $\mathbf{J}_0$ can be ignored.
2) The device is made from *nonlinear* material for which the first-order fields become related.

Assume that the relationships between the first-order fields are expressed as

$$\mathbf{J}_1 = \mathscr{J}(\mathbf{E}_1) \ , \tag{26}$$

$$\mathbf{B}_1 = \mathscr{B}(\mathbf{H}_1) \ , \tag{27}$$

$$\mathbf{D}_1 = \mathscr{D}(\mathbf{E}_1) \ , \tag{28}$$

where $\mathscr{J}$, $\mathscr{B}$, and $\mathscr{D}$ are one-to-one continuous functions defined over space coordinates only. Combining Eq. 25, in which we have now $\mathbf{D}_0 \approx 0$, with Eq. 26 gives

$$\nabla \times \mathbf{H}_1 = \mathscr{J}(\mathbf{E}_1) \ . \tag{29}$$

As the curl operator does not involve time derivatives, and $\mathscr{J}$ is defined over space coordinates, Eq. 29 says that the first-order fields $\mathbf{H}_1$ and $\mathbf{E}_1$ are related. This relation can be expressed by assuming a function $\mathscr{F}$ and we can write

$$\mathbf{E}_1 = \mathscr{F}(\mathbf{H}_1) \ . \tag{30}$$

Now, Eq. 28 can be re-expressed by using Eq. 30 as

$$\mathbf{D}_1 = \mathscr{D} \circ \mathscr{F}(\mathbf{H}_1) \ . \tag{31}$$

where the operator $\circ$ indicates a combination of two functions, $f \circ g = f(g(x))$.

Also, as $\mathscr{B}$ is a one-to-one continuous function, Eq. 27 can be re-expressed as

$$\mathbf{H}_1 = \mathscr{B}^{-1}(\mathbf{B}_1) \ . \tag{32}$$

Inserting from Eq. 32 into Eq. 31 then gives

$$\mathbf{D}_1 = \mathscr{D} \circ \mathscr{F} \circ \left[\mathscr{B}^{-1}(\mathbf{B}_1)\right] \equiv \mathscr{G}(\mathbf{B}_1) \ . \tag{33}$$

Eq. 33 predicts that an instantaneous relationship can thus be established between $\mathbf{D}_1$ and $\mathbf{B}_1$. This completes Chua's argumentation using Maxwell's equations for a quasi-static representation of the electromagnetic field quantities of a memristor.

V. Conclusion

In this paper, we surveyed key aspects of the memristor as a promising nano-device. We also introduced a SPICE macro-model for the memristor and reviewed Chua's argumentation for the memristor performing quasi-static expansion of Maxwell's equations.

Nanoelectronics not only deals with the nanometer scale, materials, and devices but implies a revolutionary change even in computing algorithms. The Von-Neumann architecture is the base architecture of all current computer systems. This architecture is not capable for carrying out computation with nano-devices and materials. There are lots of different components, such as processors, memories, drivers, actuators and so on, but they are poor at mimicking the human brain. Therefore, for the next generation of computing, choosing a suitable architecture is the first step. In fact, choosing such an architecture requires deep understanding about relevant nano-device capabilities. Obviously, different capabilities might create many opportunities as well as challenges. At present, industry has pushed nanoelectronics research for highest possible compatibility with current devices and fabricating processes. However, the memristor motivates future work in nanoelectronics and nano-computing based on its capabilities.

In this paper we addressed some possible research gaps in the area of memristor and demonstrated that futher device and circuit modelling are urgently needed. The current approach to device modelling is to introuduce a physical circuit model with a number of curve fitting parameters. However, such apporach has the limitation of requiring a large number of parameters. Initially behvaioural modelling similar to the one we have proposed in this paper can be utilised, nonetheless more modelling effort is needed to accommodate both the defect and process variation issues. An interesting follow up would be the development of mapping models based on the memristor to Neuronmorphic system and dealing with the architectural level challenges like defect-tolerant and integration into current integrated circuit technologies.

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References

[1] Roadmap, "Semiconductor Industry Association," *San Jose, CA*, 1999.
[2] R. Williams, "How We Found The Missing Memristor," *IEEE Spectrum*, vol. 45, no. 12, pp. 28–35, 2008.

[3] D. Strukov and K. Likharev, "A reconfigurable architecture for hybrid CMOS/nanodevice circuits," in *Proceedings of the 2006 ACM/SIGDA 14th international symposium on Field programmable gate arrays*, pp. 131–140, ACM New York, NY, USA, 2006.

[4] D. Strukov, "Digital architectures for hybrid cmos/nanodevice circuits," *Doctoral dissertation, Stony Brook University, Stony Brook, NY*, 2006.

[5] R. I. Bahar, D. Hammerstrom, J. Harlow, J. W. H. Joyner, D. Lau, C.and Marculescu, and M. Orailoglu, A.and Pedram, "Architectures for silicon nanoelectronics and beyond," *J. Computer*, vol. 40, no. 1, pp. 25–33, 2007.

[6] L. Chua, "Memristor-the missing circuit element," *IEEE Transactions on Circuit Theory*, vol. 18, no. 5, pp. 507–519, 1971.

[7] D. Strukov, G. Snider, D. Stewart, and R. Williams, "The missing memristor found," *Nature*, vol. 453, no. 7191, pp. 80–83, 2008.

[8] L. O. Chua, "Memristor and memristive systems symposium," 2008. `http://www.youtube.com/watch?v=QFdDPzcZwbs`.

[9] B. Widrow, A. Force, and A. Corps, "Adaptive" adaline" Neuron Using Chemical" memistors.".," *Stanford Electronics Laboratories Technical Report 1553-2*, 1960.

[10] B. Tellegen, "The gyrator, a new electric network element," *Philips Res. Rep*, vol. 3, no. 2, pp. 81–101, 1948.

[11] H. Carlin, "Singular network elements," *IEEE Transactions on Circuit Theory*, vol. 11, no. 1, pp. 67–72, 1964.

[12] T. Kraemer, "Hp memristor missing circuit element," 2008. `http://thomaskraemer.blogspot.com/2008/12/hp-memristor-missing-circuit-element.html`.

[13] L. Chua and S. Kang, "Memristive devices and systems," *Proceedings of the IEEE*, vol. 64, no. 2, pp. 209–223, 1976.

[14] S. M. Kang, "On The Modeling of Some Classes of Nonlinear Devices and Systems," *Doctoral dissertation, University of California, Berkeley*, 1975.

[15] F. Wang, "Memristor for Introductory Physics," *Arxiv preprint arXiv:0808.0286*, 2008.

[16] G. Oster, "A note on memristors," *IEEE Transactions on Circuits and Systems*, vol. 21, no. 1, pp. 152–152, 1974.

[17] J. Yang, M. Pickett, X. Li, D. Ohlberg, D. Stewart, and R. Williams, "Memristive switching mechanism for metal/oxide/metal nanodevices," 2008.

[18] Y. Joglekar, S. Wolf, D. Zinoviev, V. Ivancevic, T. Ivancevic, A. Noack, J. Diaz, A. Ezziani, D. Spiegel, K. Menou, *et al.*, "The elusive memristor: signatures in basic electrical circuits," *Arxiv preprint arXiv:0807.3994*, 2008.

[19] M. Di Ventra, Y. Pershin, and L. Chua, "Circuit elements with memory: memristors, memcapacitors and meminductors," *Arxiv preprint arXiv:0901.3682*, 2009.

[20] L. Chua, "Synthesis of new nonlinear network elements," *Proceedings of the IEEE*, vol. 56, no. 8, pp. 1325–1340, 1968.

[21] R. Fano, L. Chu, R. Adler, and J. Dreesen, *Electromagnetic Fields, Energy, and Forces*. John Wiley and Sons, New York, 1960.